On Chip Communication Architectures System On Chip Interconnect Systems On Silicon

The purpose of this book is to evaluate strategies for future system design in multiprocessor system-on-chip (MPSoC) architectures. Both hardware design and integration of new development tools will be discussed. Novel trends in MPSoC design, combined with reconfigurable architectures are a main topic of concern. The main emphasis is on architectures, design-flow, tool-development, applications and system design.

Future system-on-chip (SoC) designs require predictable, scalable and reusable on-chip interconnect architecture to increase reliability and productivity. Current bus-based interconnect architectures are inherently non-scalable, less adaptable for reuse and their reliability decreases with system size. To overcome these problems, it has been proposed to build a message passing network for on-chip communication - network-on-chip (NoC). We aim to develop a performance analysis model for the on-chip communication of a NoC system. We will use a stochastic modeling technique for performance analysis of the on-chip communication network. In our approach, the analytic model is developed using queuing theory. The router of a NoC system consists of buffers with different quality of service (QoS). The buffers can be modeled as priority queues. Their performance can be analyzed using the principles of queuing theory. The analytical results thus calculated are verified with the corresponding simulation results.

Recently the world celebrated the 60th anniversary of the invention of the first transistor. The first integrated circuit (IC) was built a decade later, with the first microprocessor designed in the early 1970s. Today, ICs are a part of nearly every aspect of our daily lives. They help us live longer and more comfortably, and do more, faster. All this is possible because of the relentless search for new materials, circuit designs, and ideas happening on a daily basis at industrial and academic institutions around the globe. Showcasing the latest advances in very-large-scale integrated (VLSI) circuits, VLSI: Circuits for Emerging Applications provides a balanced view of industrial and academic developments beyond silicon and complementary metal-oxide-semiconductor (CMOS) technology. From quantum-dot cellular automata (QCA) to chips for cochlear implants, this must-have resource: Investigates the trend of combining multiple cores in a single chip to boost performance of the overall system Describes a novel approach to enable physically unclonable functions (PUFs) using intrinsic features of a VLSI chip Examines the VLSI implementations of major symmetric and asymmetric key cryptographic algorithms, hash functions, and digital signatures Discusses nonvolatile memories such as resistive random-access memory (Re-RAM), magneto-resistive RAM (MRAM), and floating-body RAM (FB-RAM) Explores organic transistors, soft errors, photonics, nanoelectromechanical (NEM) relays, reversible computation, bioinformatics, asynchronous logic, and more VLSI: Circuits for Emerging Applications presents cutting-edge research, design architectures, materials, and uses for VLSI circuits, offering valuable insight into the current state of the art of micro- and nanoelectronics.

It is a key task of modern System-on-Chip (SoC) and Network-on-Chip (NoC) design to efficiently explore this design space regarding aspects like performance, flexibility and power consumption presumably in an early stage of the design flow in order to reduce design time and design costs. In this chapter several examples for modelling of on-chip communication using Petri Net based modelling techniques have been presented. These examples include modelling of internal processor communication and modelling of inter-processor communication using a crossbar switch fabric. For these examples deterministic and stochastic Petri Nets have been applied as modelling technique. More complex NoC communication has been modelled applying Coloured Petri Nets. The results obtained with all of these models were compared to those calculated on an FPGA based emulator. In all presented experiments the performance measures derived using these models showed a good precision compared to the results acquired using the FPGA based emulator. Furthermore, the Petri Net based results could be derived in attractively short modelling times with only moderate effort. Therefore, Petri Net based modelling of on-chip communication appears to be a very attractive approach to explore the design space of communication architectures in an early stage of the design process. DSPN based and CPN based modelling both provide specific advantages. DSPN models are suited for systems with moderate complexity such as communication systems with a small number of clients or bus based communication. The ease of modelling combined with the possibility of an analytical solution of the equations underlying the DSPN model provides a way to quickly obtain results. For more complex systems including a lot of data and complex functionalities, for example the addressing scheme and the routing algorithm in a NoC, CPN models are more adequate. DSPN based modelling of such systems is not as efficient since DSPNs do not provide a means of modelling data structures. As CPNs include data structures and allow to model complex behaviour in form of colourset and transfer functions, CPN based modelling is well suited to analyze complex on-chip communication systems. Current topics in the field of NoC communication modelling to be addressed with Petri Net based methods are locating hotspots, analyzing quality-of-service aspects (data integrity, guaranteed service, etc.) and complex adaptive routing algorithms (incl. the checking of absence of deadlocks).

Embedded Systems and Software Validation

Dynamically Configurable System-on-chip Platforms

System-level Architectures and Design Methodologies

Petri Net Based Modelling of Communication in Systems on Chip

Design Methodologies and Tools for 5G Network Development and Application

On-chip Communication Architecture Synthesis for Multi-processor Systems-on-chip

"As semiconductor technologies continues to scale, more and more cores are being integrated on the same multicore chip. This increase in complexity poses the challenge of efficient data transfer between these cores. Several on-chip network architectures are proposed to improve the design flexibility and communication efficiency of such multicore chips. However, in a larger system consisting of several multicore chips across a board or in a System-in-Package (SiP), the performance is limited by the communication among and within these chips. Such systems, most commonly found within computing modules in typical data center nodes or server racks, are in dire need of an efficient interconnection architecture. Conventional interchip communication using wireline links involve routing the data from the internal cores to the peripheral I/O ports, travelling over the interchip channels to the destination chip, and finally getting routed from the I/O to the internal cores there. This multihop communication increases latency and energy consumption while decreasing data bandwidth in a multichip system. Furthermore, the intrachip and interchip communication architectures are separately designed to maximize design flexibility. Jointly designing them could, however, improve the communication efficiency significantly and yield better solutions. Previous attempts at this include an all-photonic approach that provides a unified inter/intra-chip optical network, based on recent progress in nano-photonic technologies. Works on wireless inter-chip interconnects successfully yielded better results than their wired counterparts, but their scopes were limited to establishing a single wireless connection between two chips rather than a communication architecture for a system as a whole. In this thesis, the design of a seamless hybrid wired and wireless interconnection network for multichip systems in a package is proposed. The design utilizes on-chip wireless transceivers with dimensions spanning up to tens of centimeters. It manages to seamlessly bind both intrachip and interchip communication architectures and enables direct chip-to-chip communication between the internal cores. It is shown through cycle accurate simulations that the proposed design increases the bandwidth and reduces the energy consumption when compared to the state-of-the-art wireline I/O based multichip communications."--Abstract.

The demand for mobile broadband will continue to increase in upcoming years, largely driven by the need to deliver ultra-high definition video. 5G is not only evolutionary, it also provides higher bandwidth and lower latency than the current-generation technology. More importantly, 5G is revolutionary in that it is expected to enable fundamentally new applications with much more stringent requirements in latency and bandwidth. 5G should help solve the last-mile/last-kilometer problem and provide broadband access to the next billion users on earth at a much lower cost because of its use of new spectrum and its improvements in spectral efficiency. 5G wireless access networks will need to combine several innovative aspects of decentralized and centralized allocation looking to maximize performance and minimize signaling load. Research is currently conducted to understand the inspirations, requirements, and the promising technical options to boost and enrich activities in 5G. Design Methodologies and Tools for 5G Network Development and Application presents the enhancement methods of 5G communication, explores the methods for faster communication, and provides a promising alternative solution that equips designers with the capability to produce high performance, scalable, and adoptable communication protocol. This book provides complete design methodologies, supporting tools for 5G communication, and innovative works. The design and evaluation of different proposed 5G structures signal integrity, reliability, low-power techniques, application mapping, testing, and future trends. This book is ideal for researchers who are working in communication, networks, design and implementations, industry personnel, engineers, practitioners, academicians, and students who are interested in the evolution, importance, usage, and technology adoption for 5G applications.

This book presents an overview of the issues related to the test, diagnosis and fault-tolerance of Network on Chip-based systems. It is the first book dedicated to the quality aspects of NoC-based systems and will serve as an invaluable reference to the problems, challenges, solutions, and trade-offs related to designing and implementing state-of-the-art, on-chip communication architectures.

Abstract: Network-on-Chip (NoC) communication architectures have been recognized as the most scalable and efficient solution for on chip communication challenges in the multi-core era. Diverse demanding applications coupled with the ability to integrate billions of transistors on a single chip are some of the main driving forces behind ever increasing performance requirements towards the level that requires several tens to over a hundred of cores per chip. Small scale multicore processors so far have been a great commercial success and found applicability in many applications. Systems using multi-core processors are now the norm rather than the exception. As the number of cores or components integrated into a single system is keep increasing, the design of on-chip communication architecture is becoming more challenging. The increasing number of components in a system translates into more inter-component communication that must be handled by the on-chip communication infrastructure. Future system-on-chip (SoC) designs require predictable, scalable and reusable on-chip communication architectures to increase reliability and productivity. Current bus-based interconnect architectures are inherently non-scalable, less adaptable for reuse and their reliability decreases with system size. NoC communication guarantees scalability, high-speed, high-bandwidth communication with minimal wiring overhead and routing issues. NoCs are layered, packet-based on-chip communication networks integrated onto a single chip. NoC consists of resources and switches that are directly connected in a way that resources are able to communicate with each other by sending messages. The proficiency of a NoC to meet its design goals and budget requirements for the target application depends on its design. Often, these design goals conflict and trade-off with each other. The multi-dimensional pull of design constraints in addition to technology scaling complicates the process of NoC design in many aspects, as they are expected to support high performance and reliability along with low cost, smaller area, less time-to-market and lower power consumption. To aid in the process, this research presents design methodologies to achieve low power and high performance NoC communication architectures for nanometer SoCs.

Design Space Exploration

Integrated System-Level Modeling of Network-on-Chip enabled Multi-Processor Platforms

Designing Low Power and High Performance Network-on-Chip Communication Architectures for Nanometer SoCs

Embedded Computer Systems: Architectures, Modeling, and Simulation

Embedded Systems Handbook

5th International Workshop, SAMOS 2005, Samos, Greece, July 18-20, Proceedings

Modern embedded systems require high performance, low cost and low power consumption. Such systems typically consist of a heterogeneous collection of processors, specialized memory subsystems, and partially programmable or fixed-function components. This heterogeneity, coupled with issues such as hardware/software partitioning, mapping, scheduling, etc., leads to a large number of design possibilities, making performance debugging and validation of such systems a difficult problem. Embedded systems are used to control safety critical applications such as flight control, automotive electronics and healthcare monitoring. Clearly, developing reliable software/systems for such applications is of utmost importance. This book describes a host of debugging and verification methods which can help to achieve this goal. Covers the major abstraction levels of embedded systems design, starting from software analysis and micro-architectural modeling, to modeling of resource sharing and communication at the system level Integrates formal techniques of validation for hardware/software with debugging and validation of embedded system design flows Includes practical case studies to answer the questions: does a design meet its requirements, if not, then which parts of the system are responsible for the violation, and once they are identified, then how should the design be suitably modified?

Embedded systems are nearly ubiquitous, and books on individual topics or components of embedded systems are equally abundant. Unfortunately, for those designers who thirst for knowledge of the big picture of embedded systems there is not a drop to drink. Until now. The Embedded Systems Handbook is an oasis of information, offering a mix of basic a

This book provides comprehensive coverage of Network-on-Chip (NoC) security vulnerabilities and state-of-the-art countermeasures, with contributions from System-on-Chip (SoC) designers, academic researchers and hardware security experts. Readers will gain a clear understanding of the existing security solutions for on-chip communication architectures and how they can be utilized effectively to design secure and trustworthy systems.

The Industrial Information Technology Handbook focuses on existing and emerging industrial applications of IT, and on evolving trends that are driven by the needs of companies and by industry-led consortia and organizations. Emphasizing fast growing areas that have major impacts on industrial automation and enterprise integration, the Handbook covers topics such as industrial communication technology, sensors, and embedded systems. The book is organized into two parts. Part 1 presents material covering new and quickly evolving aspects of IT. Part 2 introduces cutting-edge areas of industrial IT. The Handbook presents material in the form of tutorials, surveys, and technology overviews, combining fundamentals and advanced issues, with articles grouped into sections for a cohesive and comprehensive presentation. The text contains 112 contributed reports by industry experts from government, companies at the forefront of development, and some of the most renowned academic and research institutions worldwide. Several of the reports on recent developments, actual deployments, and trends cover subject matter presented to the public for the first time.

Integrated Optical Interconnect Architectures for Embedded Systems

High Performance System-on-chip Communication Architectures

Architecture, Optimization, and Design Explorations

System on Chip Interconnect

Multiprocessor Systems-on-chips

International Conference on Computer Applications 2012 :: Volume 03

Such a multi-faceted synthesis framework accrues many benefits for MPSoC designs such as improved design reliability and quality, better complexity management, reduced system cost and a faster time-to-market. The experiments on several industrial strength applications demonstrate the utility of the automated and comprehensive synthesis framework for MPSoC designs.

This book constitutes the thoroughly refereed postproceedings of the First International Conference on Embedded Software and Systems, ICESS 2004, held in Hangzhou, China in December 2004. The 80 revised full papers presented together with the abstracts of 4 keynote speeches and 4 invited talks were thoroughly reviewed and selected from almost 400 submissions. The papers are organized in topical sections on distributed embedded computing, embedded systems, embedded hardware and architecture, middleware for embedded computing, mobile systems, transducer network, embedded operating system, power-aware computing, real-time system, embedded system verification and testing, and software tools for embedded systems.

Low-Power Design of Nanometer FPGAs Architecture and EDA is an invaluable reference for researchers and practicing engineers concerned with power-efficient, FPGA design. State-of-the-art power reduction techniques for FPGAs will be described and compared. These techniques can be applied at the circuit, architecture, and electronic design automation levels to describe both the dynamic and leakage power sources and enable strategies for codesign. Low-power techniques presented at key FPGA design levels for circuits, architectures, and electronic design automation, form critical, "bridge" guidelines for codesign Comprehensive review of leakage-tolerant techniques empowers designers to minimize power dissipation Provides valuable tools for estimating power efficiency/savings of current, low-power FPGA design techniques

[2]. The Cell Processor from Sony, Toshiba and IBM (STI) [3], and the Sun UltraSPARC T1 (formerly codenamed Niagara) [4] signal the growing popularity of such systems. Furthermore, Intel's very recently announced 80-core TeraFLOP chip [5] exemplifies the irreversible march toward many-core systems with tens or even hundreds of processing elements. 1.2 The Dawn of the Communication-Centric Revolution The multi-core thrust has ushered the gradual displacement of the computati- centric design model by a more communication-centric approach [6]. The large, sophisticated monolithic modules are giving way to several smaller, simpler p- cessing elements working in tandem. This trend has led to a surge in the popularity of multi-core systems, which typically manifest themselves in two distinct incarnations: heterogeneous Multi-Processor Systems-on-Chip (MPSoC) and homogeneous Chip Multi-Processors (CMP). The SoC philosophy revolves around the technique of Platform-Based Design (PBD) [7], which advocates the reuse of Intellectual Property (IP) cores in flexible design templates that can be customized accordingly to satisfy the demands of particular implementations. The appeal of such a modular approach lies in the substantially reduced Time-To- Market (TTM) incubation period, which is a direct outcome of lower circuit complexity and reduced design effort. The whole system can now be viewed as a diverse collection of pre-existing IP components integrated on a single die.

A Holistic Design Exploration

A Methodology for Interconnect Testing of Network-on-chip

Methodologies and Applications

Reconfigurable Networks-on-Chip

Network-on-Chip Security and Privacy

Communication Architectures for Systems-on-Chip

This book provides a comprehensive survey of recent progress in the design and implementation of Networks-on-Chip. It addresses a wide spectrum of on-chip communication problems, ranging from physical, network, to application layers. Specific topics that are explored in detail include packet routing, resource arbitration, error control/correction, application mapping, and communication scheduling. Additionally, a novel bi-directional communication channel NoC (BiNoC) architecture is described, with detailed explanation. Written for practicing engineers in need of practical knowledge about the design and implementation of networks-on-chip; Includes tutorial-like details to introduce readers to a diverse range of NoC designs, as well as in-depth analysis for designers with NoC experience to explore advanced issues; Describes a variety of on-chip communication architectures, including a novel bi-directional communication channel NoC. From the Foreword: Overall this book shows important advances over the state of the art that will affect future system design as well as R&D in tools and methods for NoC design. It represents an important reference point for both designers and electronic design automation researchers and developers. --Giovanni De Micheli

Parallel and distributed computing in the 1980s and 1990s had great in?uence onapplication developmentin science, engineering andbusiness computing. The improvements in computation and communication capabilities have enabled the creation of demanding applications in critical domains such as the environment, health, aerospace, and other areas of science and technology. Similarly, new classesofapplicationsareenabledbytheavailabilityofheterogeneouslarge-scale distributed systems which are becoming available nowadays (based on techno- giessuchasgridandpeer-to-peersystems).Parallelcomputingsystemsexploita large diversity of computer architectures, from supercomputers, shared-memory or distributed-memory multi processors, to local networks

and clusters of p- sonal computers. With the recent emergence of multi core architectures, parallel computing is now set to achieve " mainstream " status. Approaches that have been advocated by parallelcomputing researchersin the past are now being utilized in a number of software libraries and hardware systems that are available for everyday use. Parallel computing ideas have also come to dominate areas such as multi user gaming (especially in the development of gaming engines based on " cell " arc- tectures) – often ignored by many " serious " researchers in the past, but which now are set to have a growing user base of tens of millions across the world. In recent years, focus has also shifted to support energy e?ciency in com- tation, with some researchers proposing a new metric of performance based on Flops/Watt.

System on chips designs have evolved from fairly simple unicore, single memory designs to complex heterogeneous multicore SoC architectures consisting of a large number of IP blocks on the same silicon. To meet high computational demands posed by latest consumer electronic devices, most current systems are based on such paradigm, which represents a real revolution in many aspects in computing. The attraction of multicore processing for power reduction is compelling. By splitting a set of tasks among multiple processor cores, the operating frequency necessary for each core can be reduced, allowing to reduce the voltage on each core. Because dynamic power is proportional to the frequency and to the square of the voltage, we get a big gain, even though we may have more cores running. As more and more cores are integrated into these designs to share the ever increasing processing load, the main challenges lie in efficient memory hierarchy, scalable system interconnect, new programming paradigms, and efficient integration methodology for connecting such heterogeneous cores into a single system capable of leveraging their individual flexibility. Current design methods tend toward mixed HW/SW co-designs targeting multicore systems on-chip for specific applications. To decide on the lowest cost mix of cores, designers must iteratively map the device ' s functionality to a particular HW/SW partition and target architectures. In addition, to connect the heterogeneous cores, the architecture requires high performance complex communication architectures and efficient communication protocols, such as hierarchical bus, point-to-point connection, or Network-on-Chip. Software development also becomes far more complex due to the difficulties in breaking a single processing task into multiple parts that can be processed separately and then reassembled later. This reflects the fact that certain processor jobs cannot be easily parallelized to run concurrently on multiple processing cores and that load balancing between processing cores – especially heterogeneous cores – is very difficult.

In 2007 The Design, Automation and Test in Europe (DATE) conference celebrated its tenth anniversary. As a tribute to the chip and system-level design and design technology community, this book presents a compilation of the three most influential papers of each year. This provides an excellent historical overview of the evolution of a domain that contributed substantially to the growth and competitiveness of the circuit electronics and systems industry.

Performance Evaluation of the On-Chip Communications in a Network-On-Chip System

Embedded Software and Systems

Network-on-Chip Architectures

VLSI

Architectures and Design Methodologies

Architecture and EDA

Integrated System-Level Modeling of Network-on-Chip Enabled Multi-Processor Platforms first gives a comprehensive update on recent developments in the area of SoC platforms and ESL design methodologies. The main contribution is the rigorous definition of a framework for modeling at the timing approximate level of abstraction. Subsequently this book presents a set of tools for the creation and exploration of timing approximate SoC platform models.

This book gives a comprehensive introduction to the design challenges of MPSoC platforms, focusing on early design space exploration. It defines an iterative methodology to increase the abstraction level so that evaluation of design decisions can be performed earlier in the design process. These techniques enable exploration on the system level before undertaking time- and cost-intensive development.

Over the past decade, system-on-chip (SoC) designs have evolved to address the ever increasing complexity of applications, fueled by the era of digital convergence. Improvements in process technology have effectively shrunk board-level components so they can be integrated on a single chip. New on-chip communication architectures have been designed to support all inter-component communication in a SoC design. These communication architecture fabrics have a critical impact on the power consumption, performance, cost and design cycle time of modern SoC designs. As application complexity strains the communication backbone of SoC designs, academic and industrial R & D efforts and dollars are increasingly focused on communication architecture design. On-Chip Communication Architecures is a comprehensive reference on concepts, research and trends in on-chip communication architecture design. It will provide readers with a comprehensive survey, not available elsewhere, of all current standards for on-chip communication architectures. A definitive guide to on-chip communication architectures, explaining key concepts, surveying research efforts and predicting future trends Detailed analysis of all popular standards for on-chip communication architectures Comprehensive survey of all research on communication architectures, covering a wide range of topics relevant to this area, spanning the past several years, and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next several years.

This book provides a broad overview of current research in optical interconnect technologies and architectures. Introductory chapters on high-performance computing and the associated issues in conventional interconnect architectures, and on the fundamental building blocks for integrated optical interconnect, provide the foundations for the bulk of the book which brings together leading experts in the field of optical interconnect architectures for data communication. Particular emphasis is given to the ways in which the photonic components are assembled into architectures to address the needs of data-intensive on-chip communication, and to the performance evaluation of such architectures for specific applications.

Network-on-Chip

Runtime Adaptive System-on-Chip Communication Architecture

The Next Generation of System-on-Chip Integration

Multiprocessor Systems on Chip

The Industrial Information Technology Handbook

The Most Influential Papers of 10 Years DATE

Modeling and Simulation of Computer Networks and Systems: Methodologies and Applications introduces you to a broad array of modeling and simulation issues related to computer networks and systems. It focuses on the theories, tools, applications and uses of modeling and simulation in order to effectively optimize networks. It describes methodologies for modeling and simulation of new generations of wireless and mobiles networks and cloud and grid computing systems. Drawing upon years of practical experience and using numerous examples and illustrative applications recognized experts in both academia and industry, discuss: Important and emerging topics in computer networks and systems including but not limited to; modeling, simulation, analysis and security of wireless and mobiles networks especially as they relate to next generation wireless networks Methodologies, strategies and tools, and strategies needed to build computer networks and systems modeling and simulation from the bottom up Different network performance metrics including, mobility, congestion, quality of service, security and more... Modeling and Simulation of Computer Networks and Systems is a must have resource for network architects, engineers and researchers who want to gain insight into optimizing network performance through the use of modeling and simulation. Discusses important and emerging topics in computer networks and Systems including but not limited to; modeling, simulation, analysis and security of wireless and mobiles networks especially as they relate to next generation wireless networks Provides the necessary methodologies, strategies and tools needed to build computer networks and systems modeling and simulation from the bottom up Includes comprehensive review and evaluation of simulation tools and methodologies and different network performance metrics including mobility, congestion, quality of service, security and more

The first book to survey this emerging field in digital system design.

Over the past decade, system-on-chip (SoC) designs have evolved to address the ever increasing complexity of applications, fueled by the era of digital convergence. Improvements in process technology have effectively shrunk board-level components so they can be integrated on a single chip. New on-chip communication architectures have been designed to support all inter-component communication in a SoC design. These communication architecture fabrics have a critical impact on the power consumption, performance, cost and design cycle time of modern SoC designs. As application complexity strains the communication backbone of SoC designs, academic and industrial R&D efforts and dollars are increasingly focused on communication architecture design. On-Chip Communication Architecures is a comprehensive reference on concepts, research and trends in on-chip communication architecture design. It will provide readers with a comprehensive survey, not available elsewhere, of all current standards for on-chip communication architectures. A definitive guide to on-chip communication architectures, explaining key concepts, surveying research efforts and predicting future trends Detailed analysis of all popular standards for on-chip communication architectures Comprehensive survey of all research on communication architectures, covering a wide range of topics relevant to this area, spanning the past several years, and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next several years

"This 10-volume compilation of authoritative, research-based articles contributed by thousands of researchers and experts from all over the world emphasized modern issues and the presentation of potential opportunities, prospective solutions, and future directions in the field of information science and technology"--Provided by publisher.

Modeling, Analysis and Optimization of Network-on-Chip Communication Architectures

Encyclopedia of Information Science and Technology, Third Edition

An Interconnection Architecture for Seamless Inter and Intra-chip Communication Using Wireless Links

Low-Power Design of Nanometer FPGAs

7th International Conference, ICA3PP 2007, Hangzhou, China, June 11-14, 2007, Proceedings

Algorithms and Architectures for Parallel Processing

Limitations of bus-based interconnections related to scalability, latency, bandwidth, and power consumption for supporting the related huge number of on-chip resources result in a communication bottleneck. These challenges can be efficiently addressed with the implementation of a network-on-chip (NoC) system. This book gives a detailed analysis of various on-chip communication architectures and covers different areas of NoCs such as potentials, architecture, technical challenges, optimization, design explorations, and research directions. In addition, it discusses current and future trends that could make an impactful and meaningful contribution to the research and design of on-chip communications and NoC systems.

A presentation of state-of-the-art approaches from an industrial applications perspective, Communication Architectures for Systems-on-Chip shows professionals, researchers, and students how to attack the problem of data communication in the manufacture of SoC architectures. With its lucid illustration of current trends and research improving the performance, quality, and reliability of transactions, this is an essential reference for anyone dealing with communication mechanisms for embedded systems, systems-on-chip, and multiprocessor architectures—or trying to overcome existing limitations. Exploring architectures currently implemented in manufactured SoCs—and those being proposed—this book analyzes a wide range of applications, including: Well-established communication buses Less common networks-on-chip Modern technologies that include the use of carbon nanotubes (CNTs) Optical links used to speed up data transfer and boost both security and quality of service (QoS) The book's contributors pay special attention to newer problems, including how to protect transactions of critical on-chip information (personal data, security keys, etc.) from an external attack. They examine mechanisms, revise communication protocols involved, and analyze overall impact on system performance.

Traditionally, design space exploration for Systems-on-Chip (SoCs) has focused on the computational aspects of the problem at hand. However, as the number of components on a single chip and their performance continue to increase, the communication architecture plays a major role in the area, performance and energy consumption of the overall system. As a result, a shift from computation-based to communication-based design becomes mandatory. Towards this end, network-on-chip (NoC) communication architectures have emerged recently as a promising alternative to classical bus and point-to-point communication architectures. In this dissertation, we study outstanding research problems related to modeling, analysis and optimization of NoC communication architectures. More precisely, we present novel design methodologies, software tools and FPGA prototypes to aid the design of application-specific NoCs.

This book constitutes the refereed proceedings of the 5th International Workshop on Systems, Architectures, Modeling, and Simulation, SAMOS 2005, held in Samos, Greece in July 2005. The 49 revised full papers presented were thoroughly reviewed and selected from 114 submissions. The papers are organized in topical sections on reconfigurable system design and implementations, processor architectures, design and simulation, architectures and implementations, system level design, and modeling and simulation.

Hardware Design and Tool Integration

On-chip Communication

Design, Automation, and Test in Europe

Modeling and Simulation of Computer Networks and Systems

Multiprocessor System-on-Chip

Development and Verification of System-on-a-chip Communication Architecture

Addresses the Challenges Associated with System-on-Chip Integration Network-on-Chip: The Next Generation of System-on-Chip Integration examines the current issues restricting chip-on-chip communication efficiency, and explores Network-on-chip (NoC), a promising alternative that equips designers with the capability to produce a scalable, reusable, and high-performance communication backbone by allowing for the integration of a large number of cores on a single system-on-chip (SoC). This book provides a basic overview of topics associated with NoC-based design: communication infrastructure design, communication methodology, evaluation framework, and mapping of applications onto NoC. It details the design and evaluation of different proposed NoC structures, low-power techniques, signal integrity and reliability issues, application mapping, testing, and future trends. Utilizing examples of chips that have been implemented in industry and academia, this text presents the full architectural design of components verified through implementation in industrial CAD tools. It describes NoC research and developments, incorporates theoretical proofs strengthening the analysis procedures, and includes algorithms used in NoC design and synthesis. In addition, it considers other upcoming NoC issues, such as low-power NoC design, signal integrity issues, NoC testing, reconfiguration, synthesis, and 3-D NoC design. This text comprises 12 chapters and covers: The evolution of NoC from SoC—its research and developmental challenges NoC protocols, elaborating flow control, available network topologies, routing mechanisms, fault tolerance, quality-of-service support, and the design of network interfaces The router design strategies followed in NoCs The evaluation mechanism of NoC architectures The application mapping strategies followed in NoCs Low-power design techniques specifically followed in NoCs The signal integrity and reliability issues of NoC The details of NoC testing strategies reported so far The problem of synthesizing application-specific NoCs Reconfigurable NoC design issues Direction of future research and development in the field of NoC Network-on-Chip: The Next Generation of System-on-Chip Integration covers the basic topics, technology, and future trends relevant to NoC-based design, and can be used by engineers, students, and researchers and other industry professionals interested in computer architecture, embedded systems, and parallel/distributed systems.

Generally, the performance of a digital system today is limited by its communication or interconnection, not by its logic or memory. In a high-end system today, most of the clock cycles are spent on wire delay, not gate delay. For a deep sub-micron technology system-on-chip (SoC) consisting of hundreds of cores, communication is one of the bottle-necks to meet performance requirements. Network-on-chip (NoC) is one of the communication architectures for future SoC's. NoC is reusable, scalable and supports parallel communication at the expense of more design complexity. Testability of NoC guarantees the proper operation of the communication architecture. Incorporating testability at the design level enables to implement better test strategies to reduce test time. Interconnect is one of the major components of the NoC architecture. In this thesis, we adapt a distributed routing methodology to the NoC. The methodology reduces the design complexity, improves the performance of the NoC, and also enables to incorporate interconnect testing with minimum design overhead by using the extra address space. A priority-based approach is developed to derive the minimum number of configurations for testing interconnects for the 2D mesh NoC. This approach reduces the redundancy in testing interconnects, and thus test cost. Further, theoretical analysis demonstrate that only two test configurations are required to test all interconnects of any (m x n) 2D mesh NoC with zero redundancy.

Reliability, Availability and Serviceability of Networks-on-Chip

Circuits for Emerging Applications

COMMSYN

First International Conference, ICESS 2004, Hangzhou, China, December 9-10, 2004, Revised Selected Papers

Multicore Systems On-Chip: Practical Software/Hardware Design

On-Chip Communication Architectures